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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/021,782	12/18/2001	Cyrus E. Tabery	50432-293	1966

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EXAMINER	
ISAAC, STANETTA D	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 05/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/021,782	TABERY ET AL.	
	Examin r	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE f this communication appears on th c ver sheet with th correspondence address --

P ri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-10* is/are allowed.

6)☒ Claim(s) *1-4,11,12 and 14* is/are rejected.

7)☒ Claim(s) *5 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 April 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the *REQUEST FOR REINSTATEMENT OF APPEAL*, filed on 02/05/04, PROSECUTION IS HEREBY REOPENED.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1, 3, 4, 11, 12, and 14 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. US Patent 6,242,292.

4. Yamazaki discloses the semiconductor method as claimed. See **FIGS. 1-6B**, where Pertaining to claims 1 and 11, Yamazaki teaches a method of manufacturing a semiconductor device, comprising the steps of:

Step 1) "forming a gate electrode over the substrate;"

See figures **5, 6A** and **6B** where these figures illustrate patterns of TFTs having a peripheral circuit **(51)** and a pixel circuit **(52)**, and as stated under **col. 9, lines 5-10 and 31**, the gate electrode is discussed as well as the substrate **(11)**. The gate is used as a mask on the substrate for subsequent implantation.

Step 2) "introducing ions into the substrate to form source/drain regions in the substrate proximate to the gate electrode;"

See figures **5, 6A** and **6B**, and as stated under **col. 9, lines 27-33**, where it specifically states "an impurity ion for providing one conductivity type... is doped into source and drain regions by ion doping or plasma doping in a self-alignment using the gate electrode as a mask,"

Step 3) "activating a portion of the source/drain regions by laser thermal annealing using a laser;" In claim 11 specifically, "...using a pulse of laser energy..."

As stated in **col. 7, lines 50-60** and **col. 9, lines 24-50**, the process of the prior art is specifically drawn to activating the source/drain regions, where an annealing process is performed to activate the impurity ion introduced into the substrate to form the source/drain regions proximate the gate electrode. Specifically, as stated in **col. 9, lines 37-44**, "Annealing for activating the impurity ion is required." and, "The annealing process for the above purpose is conducted by irradiation of laser light." In addition, stated in **col. 7, lines 56-60**, are the laser energy and the number of pulses.

Step 4) "moving the laser and the substrate relative to one another;"

As stated in **col. 2, lines 11-16**, a definition of scanning is provided by the prior art of record, where scanning means that "the linear laser is superposedly irradiated while, displaced

little by little", where the width of the laser beam exceeds the length of the substrate to be processed and where the scanning takes place relative to the substrate.

Furthermore, an interview dated May 20, 2003 was conducted in which the examiner asked the Attorney-of-Record for clarity regarding the limitation of "moving the laser and the substrate relative to one another". The Attorney-of-Record Scott Paul, replied that "it is relative to the frame of reference, for example, the laser can be stationary and the substrate can be moving." Because of the Attorney-of-Record's reply, the examiner was, and is lead to take the broadest interpretation of the claim language and by the previous statements in sections (a)-(d), was able to conclude that the prior art of record teaches that the substrate is moving and the laser is stationary, implying that they are moving relative to one another.

Step 5) "activating another portion of the source/drain regions by laser thermal annealing using the laser," In claim 11 specifically, "... using another pulse of laser energy from the laser"

(a) As stated in **col. 7, lines 50-60** and **col. 9, lines 24-50**, the process of the prior art is specifically drawn to activating the source/drain regions, where an annealing process is performed to activate the impurity ion introduced into the substrate to form the source/drain regions proximate the gate electrode. Specifically, as stated in **col. 9, lines 37-44**, "Annealing for activating the impurity ion is required." And, "The annealing process for the above purpose is conducted by irradiation of laser light."

(b) Further, as stated in **col. 8, lines 47-62, col. 10, lines 1-6**, "The linear laser light is irradiated while the direction of the source and drain regions of the TFT is coincident with the line direction of the linear laser light, whereby the crystal state in the carrier moving direction can be made uniform." This statement confirms "activating another portion of the source/drain

regions by laser thermal annealing using a laser", since the source and drain regions coincide with the line direction of the laser, the carriers move in a region having uniform crystallinity where by connecting the source and drain regions of each TFT, high mobility regarding the electrical characteristics of the TFTs can be obtained. Additionally, since the laser beam is a scanning beam, it is inherent that the beam will activate "another portion" or different portions of the source/drain regions as the beam moves along the substrate. See **col. 8, lines 30-54**; **col. 9, lines 44-50** and **58-67**; **col. 10, lines 1-5** and **FIG. 5**, wherein the laser moves over the transistor source/drain regions to form crystallinity between the source/drain regions.

(c) finally, stated in **col. 7, lines 56-60**, addresses the laser energy and the number of pulses (pulse width 30 ns, 30 pulses/s). It is inherent that since the laser beam is a scanning beam, the beam will activate another portion of the source/drain regions using another pulse of laser energy as the beam moves over the source/drain region.

Step 6) "wherein the movement of the laser and substrate relative to one another is continuous between and during the steps of activating the portion of the source/drain regions and activating the other portion of the source/drain regions." In Claim 11 specifically, "...after each pulse of laser energy and each portion of the source/drain regions receives more than one single pulse of energy..."

(a) As stated under **col. 7, lines 50-55**, "the substrate (sample) on which the silicon film is formed is placed on the stage and the laser light is irradiated onto the whole surface of the substrate by moving the stage at 2mm/s." This statement confirms "movement as the laser and the substrate is relative to one another... is continuous" as claimed in applicant's invention.

(b) Additionally, see figures **1, 2** and **5**, which illustrate the laser beam moving in a lateral direction and see **col. 6 lines 29-40**, for confirmation that the laser light is irradiated onto the whole surface of the substrate by moving the substrate in one direction.

(c) Further, as stated in **col. 2**, lines **11-16**, a definition of scanning is provided by the prior art of record, where scanning means that the linear beam is superposedly irradiated while, displaced little by little, which also confirms continuous movement between the laser and the substrate, where the width of the laser beam exceeds the length of the substrate to be processed and where the scanning takes place relative to the substrate.

(e) Finally, as stated in **col. 10, lines 1-6**, "The linear laser light is irradiated while the direction of the source and drain regions of the TFT is coincident with the line direction of the linear laser light, whereby the crystal state in the carrier moving direction can be made uniform." This statement also confirms that "activating a portion of the source/drain regions by laser thermal annealing using a laser", is performed in continuous movement.

5. Pertaining to claim 3, Yamazaki teaches "the invention according to claim 1, wherein each portion of the source/drain regions receives more than one single pulse of energy from the laser." As stated in **col. 7, lines 50-60** the number of pulses used for the irradiation process being performed is 30 pulses/s and **col. 9, lines 24-50** shows that the activation process uses the number of pulses to anneal the source/drain regions.

6. Pertaining to claims 4 and 12, Yamazaki teaches the invention according to claims 1 and 11, "wherein each pulse from the laser respectively irradiates non-identical portions of the source/drain regions." Please refer back to the statements disclosed pertaining to claims 1 and 11, with regards to the confirmation of continuous movement of the laser and substrate relative to one another (see **steps 4-6** as previously outlined). With these statements, it is confirmed that the portions of the source/drain regions must be irradiating "non-identical portions " simply because of the continuous movement of the laser and the substrate relative to one another to form connections of the source and drain regions of the TFTs.

7. Pertaining to claim 14, Yamazaki teaches "the invention according to claim 11, wherein the laser and the substrate move relative to one another at a constant velocity." Please refer back to the statements disclosed pertaining to claims 1 and 11, with regards to the confirmation of continuous movement of the laser and substrate relative to one another (see **steps 4-6** as previously outlined), in addition, as specifically stated in **col. 7, lines 50-55,** that the substrate is placed on a stage and is moved at "2 mm/s" which a constant velocity, confirms continuous movement "at a constant velocity." Such that regions are annealed in a consistent manner **(col. 8, lines 45-62)**

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al. US Patent 6,242,292 in view of Ino et al. US Patent 6,248,606.

10. Yamazaki teaches the semiconductor method substantially as claimed. Yamazaki the steps as follows:

Step 1) "forming a gate electrode over the substrate;"

Step 2) "introducing ions into the substrate to form source/drain regions in the substrate proximate to the gate electrode;"

Step 3) "activating a portion of the source/drain regions by laser thermal annealing using a laser;" In claim 11 specifically, "...using a pulse of laser energy..."

Step 4) "moving the laser and the substrate relative to one another;"

Step 5) "activating another portion of the source/drain regions by laser thermal annealing using the laser," In claim 11 specifically, "... using another pulse of laser energy from the laser"

Step 6) "wherein the movement of the laser and substrate relative to one another is continuous between and during the steps of activating the portion of the source/drain regions and activating the other portion of the source/drain regions." In Claim 11 specifically, "...after each pulse of laser energy and each portion of the source/drain regions receives more than one single pulse of energy..."

11. As stated in **col. 7, lines 50-55**, Yamazaki teaches applying "more than one single pulse of energy from the laser" to "each portion of the source/drain regions".

12. However, Yamazaki fails to teach the step of "the invention according to claim 1, wherein each portion of the source/drain regions receives no more than one single pulse of energy from the laser."

13. See figures **1, 2** and as stated in **col. 1, lines 35-48**, where Ino teaches the above step of "wherein each portion of the source/drain regions receives no more than one single pulse..." as stated "...the semiconductor film **103**", "is irradiated by the laser beam onto the whole surface of the semiconductor thin film while scanning the laser beam **105** or shifting the laser-irradiation area stepwisely." Where each area receives "one-shot laser irradiation of laser..."

14. In view of Ino, it would have been obvious to one of ordinary skill in the art to incorporate the teachings of Ino into the teachings of Yamazaki because, as taught in the conventional art it is known to use a "one-shot laser irradiation with a laser" where specifically stated in **col. 1, lines 38-42**, "In the conventional method, the output power of the laser beam is limited to a small level, and thus the maximum area which can be irradiated with one-shot irradiation with a laser is limited to a narrow area about 100 μm^2." In addition, Ino explains in **col. 1, lines 55-67**, and **col. 2**, lines **1-8**, problems that occur the due to the use of this conventional technique.

Allowable Subject Matter

15. Claims 5 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

16. Claims 6-10 are allowed.

17. The following is an examiner's statement of reasons for allowance: Applicant's independent claim 6 is allowed over the prior art of record because none teach or render obvious a method of manufacturing a semiconductor device, comprising the steps of: wherein a spot area of the laser on the substrate is less than 50 millimeters^2. See **Yamazaki et al**. US Patent

6,242,292 discloses a method of manufacturing a semiconductor device, however fails the step where the spot area of the laser on the substrate is less than 50 millimeters^2.

18. All dependent claims are also rendered allowable over the prior art of record.

19. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

20. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

21. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on 571-272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

22. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
May 3, 2004

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